[0049] What is claimed is:

1. A system comprising:

at least two processing units embedded on a chip able to communicate with each other and to generally independently control access to data from memory on said chip.

2. A system according to claim 1 and further comprising at least one first in first out (FIFO) unit used by said processing units to transfer data therebetween.

3. A system according to claim 2 and further comprising a data flow control unit able to control data transfer.

4. A system according to claim 1 wherein said processing units are central processing units (CPUs).

5. A system according to claim 1 and further comprising at least two asynchronous clocks controlling said at least two processing units.

6. A system according to claim 1 wherein one of said processing units is able to process media access control (MAC) commands and another of said processing units is able to process physical layer device (PHY) commands of a networking protocol.

7. A system comprising:

at least two CPUs embedded on a chip able to communicate with each other and to asynchronously control reading and writing of data to and from memory on said chip.

8. A system according to claim 7 and further comprising at least one FIFO unit used by said CPUs to transfer data therebetween.

9. A system according to claim 7 and further comprising a control unit to control data transfer.

10. A system according to claim 7 and further comprising at least two asynchronous clocks controlling said at least two CPUs.

11. A system according to claim 7 wherein one of said CPUs is able to process MAC commands and another of said CPUs is able to process PHY commands of a networking protocol.

12. A system comprising:

at least two processing units embedded on a chip able to asynchronously transfer data therebetween.

13. A system according to claim 12 wherein said processing units are CPUs.

14. A system according to claim 12 and further comprising at least one FIFO unit used by said processing units to transfer data therebetween.

15. A system according to claim 14 and further comprising a control unit to control data transfer.

16. A system according to claim 12 wherein one of said processing units is able to process MAC commands and another of said processing units is able to process PHY commands of a networking protocol.

17. An apparatus comprising:

a FIFO unit able to receive data from a first random access memory (RAM) accessible by a first CPU embedded on a chip and able to write said data to a second RAM accessible by a second CPU embedded on said chip.

18. An apparatus according to claim 17, further comprising at least one control unit able to control data flow to and from said FIFO unit.

19. An apparatus according to claim 18 wherein said at least one control unit is a direct memory access unit (DMA).

20. An apparatus according to claim 18, wherein said at least one control unit comprises at least one read channel able to control receipt of said data.

21. An apparatus according to claim 18, wherein said at least one control unit comprises at least one write channel able to control transmission of said data.

22. An apparatus according to claim 17, further comprising a register accessible by said first CPU and said second CPU.

23. An apparatus according to claim 17 wherein said first CPU is able to process MAC commands and said second CPU is able to process PHY commands of a networking protocol.

24. A chip having a FIFO unit, a first memory, a second memory, a first processing unit, and a second processing unit all embedded thereon wherein said FIFO unit is able to receive data from said first memory accessible by said first processing unit and able to write said data to said second memory accessible by said second processing unit.

25. A chip according to claim 24 wherein said first processing unit and said second processing unit are CPUs.

26. A chip according to claim 24 wherein said first memory and said second memory are RAM.

27. A chip according to claim 24 and further comprising a register accessible by said first processing unit and said second processing unit.

28. A system comprising:

at least one first FIFO unit able to receive a first data from at least one first memory accessible by at least one first processing unit embedded on a chip and able to write said first data to at least one second memory accessible by at least one second processing unit embedded on said chip; and

at least one second FIFO unit able to receive a second data from said second memory and able to write said second data to said first memory.

29. A system according to claim 28 wherein said first memory and said second memory are RAM.

30. A system according to claim 28 wherein said first processing unit and said second processing unit are CPUs.

31. A system according to claim 28, further comprising at least one control unit able to control data flow to and from said at least one first FIFO unit and said at least one second FIFO unit.

32. A system according to claim 31 wherein said at least one control unit comprises at least one read channel able to control receipt of said data.

33. A system according to claim 31 wherein said at least one control unit comprises at least one write channel able to control transmission of said data.

34. A system according to claim 28, further comprising a common register accessible by said first memory and said second memory.

35. A system according to claim 28 and further comprising at least two asynchronous clocks controlling said at least two processing units.

36. A method comprising:

first enabling at least one first CPU embedded on a chip to control writing of data to at least one FIFO generally concurrently with second

enabling at least one second CPU embedded on said chip to control reading of said data from said at least one FIFO.

37. A method according to claim 36, wherein said first enabling comprises any of the actions selected from the group consisting of:

instructing an apparatus to transmit data;

checking if said at least one FIFO is full before said writing;

checking if all of said data has been written; and

transmitting a signal.

38. A method according to claim 36, wherein said second enabling comprises any of the actions selected from the group consisting of:

instructing an apparatus to receive data;

checking if said at least one FIFO is empty before said reading;

checking if all data has been read;

receiving a signal; and

transmitting a signal.

39. A method comprising:

enabling a first processing unit embedded on a chip to write data to a FIFO unit from a first memory; and

enabling a second processing unit embedded on said chip to read said data from said FIFO unit and write said data to a second memory.

40. A method according to claim 39 wherein said first processing unit and said second processing unit are CPUs.

41. A method according to claim 39 wherein said first memory and said second memory are RAM.

42. A system comprising:

at least one first CPU embedded on a chip able to control reading of data from a first memory on said chip; and

at least one second CPU embedded on said chip able to control writing of said data to a second memory on said chip generally simultaneously with said reading.

43. A system according to claim 42 and further comprising at least one FIFO unit used by said first CPU and said second CPU to transfer data therebetween.

44. A system according to claim 42 and further comprising at least one control unit able to control said reading of said data and said writing of said data.

45. A system according to claim 42 and further comprising a register accessible by said first CPU and said second CPU.

46. A system according to claim 42 wherein said first CPU and said second CPU are able to process commands of a networking protocol.

47. A system according to claim 42 and further comprising at least two asynchronous clocks controlling said at least one first and at least one second CPU.

48. A system comprising:

communication means for enabling a first CPU embedded on a chip to send data to a second CPU embedded on said chip; and

means for enabling said first and said second CPU to access memory generally independently of each other.

49. A system according to claim 48 and further comprising a register accessible by said first CPU and said second CPU.

50. A system according to claim 48 and further comprising at least one FIFO unit used by said first CPU and said second CPU to transfer data therebetween.

51. A system according to claim 48 wherein said communications means is able to process networking protocol commands.

52. A chip comprising instructions for at least two processing units embedded on said chip to asynchronously control reading and writing of data to and from memory on said chip.

53. A chip comprising instructions for at least two processing units embedded on said chip to generally independently control access to data from memory on said chip.